Code No: R1631043 **R16** SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2019

DIGITAL IC APPLICATIONS

(**Common to** Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	Define CMOS Logic levels.	[2M]
	b)	Differentiate between Functions and Procedures in VHDL.	[2M]
	c)	Explain the library structure of VHDL.	[2M]
	d)	What are the advantages of ECL?	[3M]
	e)	Explain about half subtractor.	[3M]
	f)	Explain a ring counter.	[2M]

PART -B

2.	a)	How that at a given power-supply voltage, an FCT-type I_{CCD} specification can be derived from an HCT/ACT-type C_{PD} specification, and vice versa.	[7M]
	b)	Quantitatively explain the power dissipation of CMOS circuit.	[7M]
3.	a)	Explain wait, if, case statements in VHDL.	[7M]
	b)	With an example, explain structural and data flow style of modeling.	[7M]
4.	a)	Explain the blocks inside a logic synthesizer.	[7M]
	b)	Write a VHDL program for4x2 Encoder and 2x4 decoder.	[7M]
5.	a)	Write the VHDL architecture for a dual priority encoder.	[7M]
	b)	Draw the circuit and explain the operation of binary adder-subtractor.	[7M]
6.	a)	Explain the operation of 8bit serial in parallel our shift register and give VHDL description.	[7M]
	b)	Explain the operation of MOD-10 Counter.	[7M]
7.	a)	Describe about 74x74 D flip-flop and write VHDL program with preset and clear.	[7M]
	b)	Give a code in VHDL of a serial adder.	[7M]

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