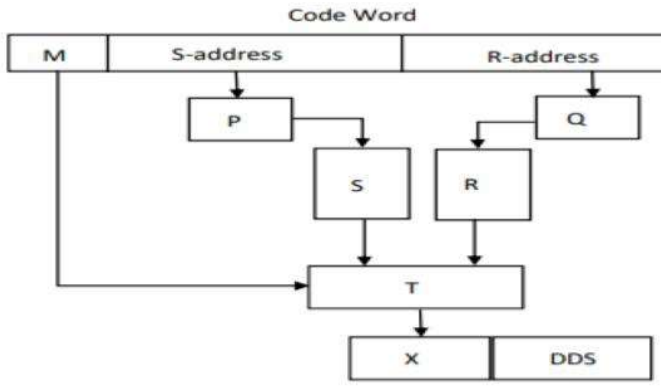
# GATE 2024 CSE Daily Practice Questions

***Question 1: Consider a digital display system (DDS) shown in the figure that displays the contents of register X. A 16-bit code word is used to load a word in X, either from S or from R. S is a 1024-word memory segment and R is a 32-word register file. Based on the value of mode bit M, T selects an input word to load in X. P and Q interface with the corresponding bits in the code word to choose the addressed word. Which one of the following represents the functionality of P, Q, and T?***




| | | | |
|---|---|---|---|
| (A) | P is 10:1 multiplexer; | Q is 5:1 multiplexer; | T is 2:1 multiplexer |
| (B) | P is 10:$2^{10}$ decoder; | Q is 5:$2^{5}$ decoder; | T is 2:1 encoder |
| (C) | P is 10:$2^{10}$ decoder; | Q is 5:$2^{5}$ decoder; | T is 2:1 multiplexer |
| (D) | P is 1:10 de-multiplexer; | Q is 1:5 de-multiplexer; | T is 2:1 multiplexer |

***Question 2: Which one of the following statements is FALSE?***

*(A) The TLB performs an associative search in parallel on all its valid entries using page number of incoming virtual address.*

*(B) If the virtual address of a word given by CPU has a TLB hit, but the subsequent search for the word results in a cache miss, then the word will always be present in the main memory.*

*(C) The memory access time using a given inverted page table is always same for all incoming virtual addresses.*

*(D) In a system that uses hashed page tables, if two distinct virtual addresses V1 and V2 map to the same value while hashing, then the memory access time of these addresses will not be the same.*

*Question 3: Consider four processes P, Q, R, and S scheduled on a CPU as per round robin algorithm with a time quantum of 4 units. The processes arrive in the order P, Q, R, S, all at time t = 0. There is exactly one context switch from S to Q, exactly one context switch from R to Q, and exactly two context switches from Q to R. There is no context switch from S to P. Switching to a ready process after the termination of another process is also considered a context switch. Which one of the following is*

*NOT possible as CPU burst time (in time units) of these processes?*

*(A) P = 4, Q = 10, R = 6, S = 2*

*(B) P = 2, Q = 9, R = 5, S = 1*

*(C) P = 4, Q = 12, R = 5, S = 4*

*(D) P = 3, Q = 7, R = 7, S = 3*

*Question 4: Suppose two hosts are connected by a point-to-point link and they are configured to use Stop-and-Wait protocol for reliable data transfer. Identify in which one of the following scenarios, the utilization of the link is the lowest.*

*(A) Longer link length and lower transmission rate*

*(B) Longer link length and higher transmission rate*

*(C) Shorter link length and lower transmission rate*

*(D) Shorter link length and higher transmission rate*

*Question 5: Which of the following statements is/are TRUE with respect to deadlocks?*

*(A) Circular wait is a necessary condition for the formation of deadlock.*

*(B) In a system where each resource has more than one instance, a cycle in its wait-for graph indicates the presence of a deadlock.*

*(C) If the current allocation of resources to processes leads the system to unsafe state, then deadlock will necessarily occur.*

*(D) In the resource-allocation graph of a system, if ev*

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