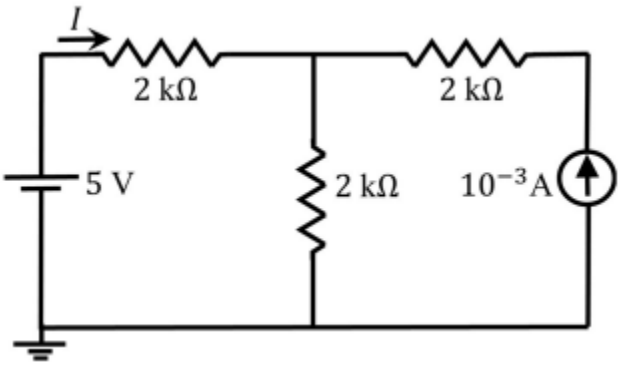
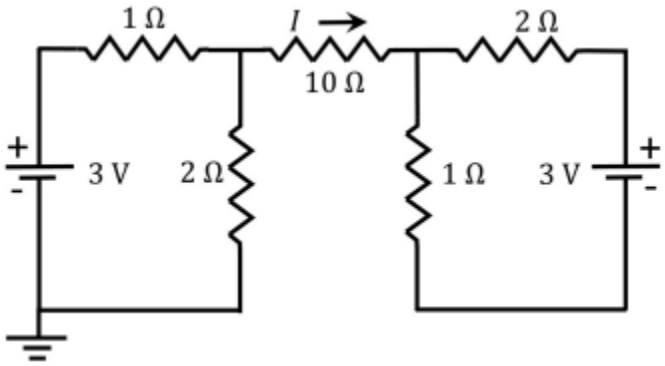
Q1) The current I in the circuit shown is _____.



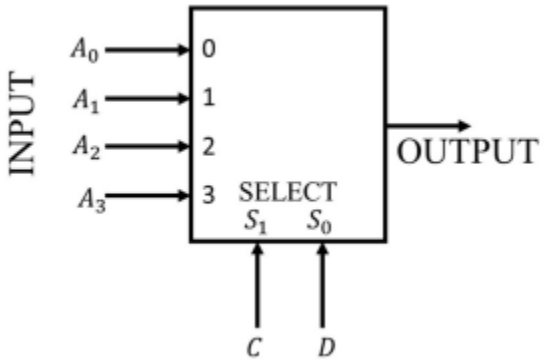
(A) 1.25×10^{-3}A
(B) 0.75×10^{-3}A
(C) -0.5×10^{-3}A
(D) 1.16×10^{-3}A

Q2) Consider the circuit shown in the figure. The current I flowing through the 10 Ω resistor is _____.



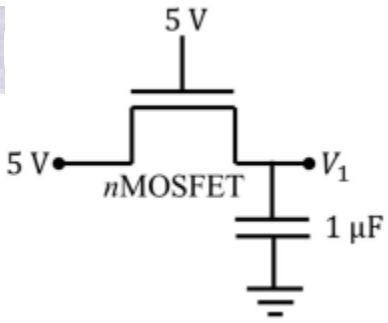
(A) 1 A
(B) 0 A
(C) 0.1 A
(D) -0.1 A

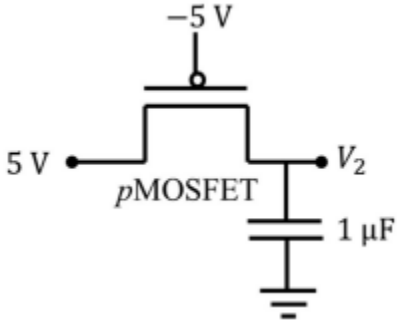
Q3) Consider the 2-bit multiplexer (MUX) shown in the figure. For OUTPUT to be the XOR of C and D, the values for A_0, A_1, A_2, and A_3 are _____.



(A) $A_0 = 0, A_1 = 0, A_2 = 1, A_3 = 1$
(B) $A_0 = 1, A_1 = 0, A_2 = 1, A_3 = 0$
(C) $A_0 = 0, A_1 = 1, A_2 = 1, A_3 = 0$
(D) $A_0 = 1, A_1 = 1, A_2 = 0, A_3 = 0$

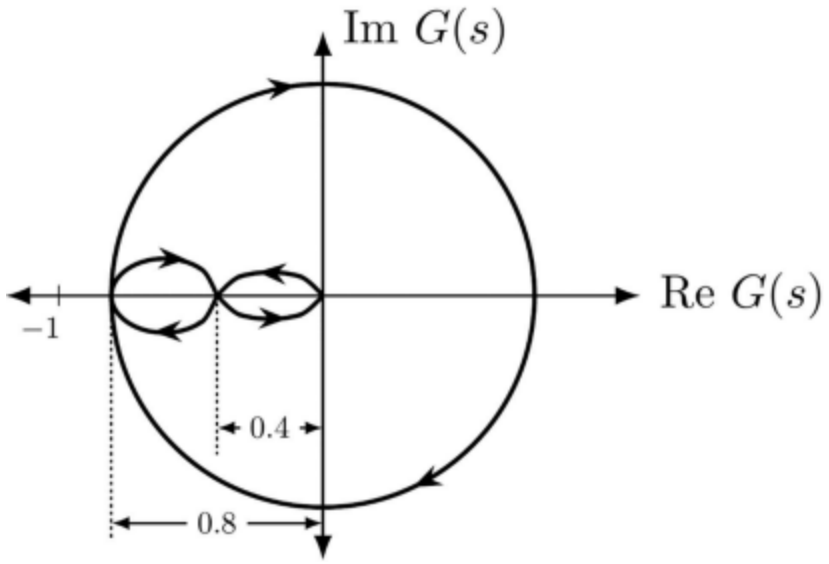
Q4) The ideal long channel nMOSFET and pMOSFET devices shown in the circuits have threshold voltages of 1 V and −1 V, respectively. The MOSFET substrates are connected to their respective sources. Ignore leakage currents and assume that the capacitors are initially discharged. For the applied voltages as shown, the steady state voltages are_____.





(A) $V_1 = 5$ V, $V_2 = 5$ V
(B) $V_1 = 5$ V, $V_2 = 4$ V
(C) $V_1 = 4$ V, $V_2 = 5$ V
(D) $V_1 = 4$ V, $V_2 = -5$ V

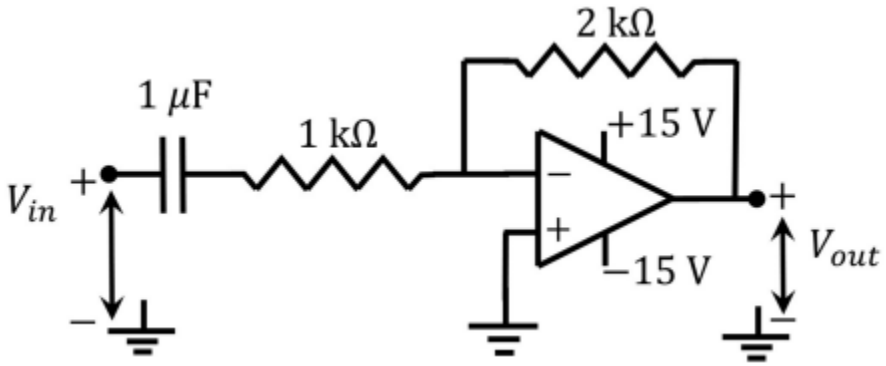
Q5) Consider a closed-loop control system with unity negative feedback and $KG(s)$ in the forward path, where the gain K = 2. The complete Nyquist plot of the transfer function $G(s)$ is shown in the figure. Note that the Nyquist contour has been chosen to have the clockwise sense. Assume $G(s)$ has no poles on the closed right-half of the complex plane. The number of poles of the closed-loop transfer function in the closed right-half of the complex plane is _____.



(A) 0
(B) 1
(C) 2
(D) 3

Q6) In a circuit, there is a series connection of an ideal resistor and an ideal capacitor. The conduction current (in Amperes) through the resistor is $2\sin(t + \pi/2)$. The displacement current (in Amperes) through the capacitor is _____.
(A) $2\sin(t)$
(B) $2\sin(t + \pi)$
(C) $2\sin(t + \pi/2)$
(D) 0

Q7) An ideal OPAMP circuit with a sinusoidal input is shown in the figure. The 3 dB frequency is the frequency at which the magnitude of the voltage gain decreases by 3 dB from the maximum value. Which of the options is/are correct?



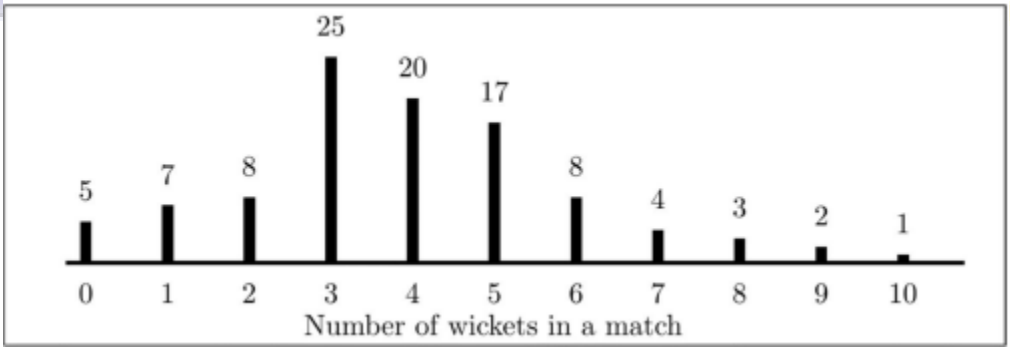
(A) The circuit is a low pass filter.
(B) The circuit is a high pass filter.

(C) The 3 dB frequency is 1000 rad/s.
(D) The 3 dB frequency is 1000/3 rad/s

Q8) Select the Boolean function(s) equivalent to $x + yz$, where x, y, and z are Boolean variables, and + denotes logical OR operation
(A) $x + z + xy$
(B) $(x + y)(x + z)$
(C) $x + xy + yz$
(D) $x + xz + x$y

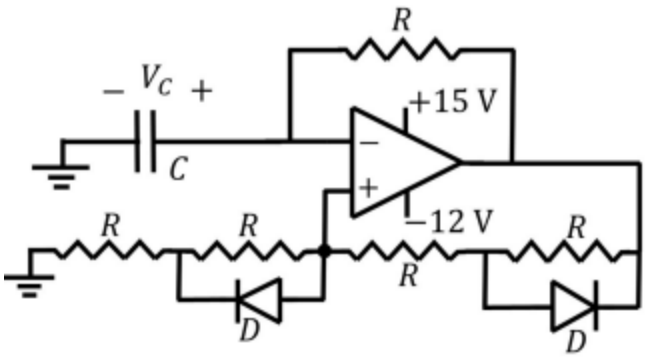
Q9) Select the correct statement(s) regarding CMOS implementation of NOT gates
(A) Noise Margin High (NM_u) is always equal to the Noise Margin Low (NM_L), irrespective of the sizing of transistors.
(B) Dynamic power consumption during switching is zero.
(C) For a logical high input under steady state, the nMOSFET is in the linear regime of operation.
(D) Mobility of electrons never influences the switching speed of the NOT gate.

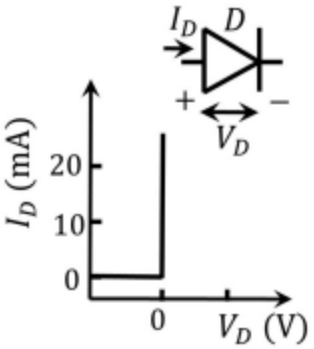
Q10) The bar graph shows the frequency of the number of wickets taken in a match by a bowler in her career. For example, in 17 of her matches, the bowler has taken 5 wickets each. The median number of wickets taken by the bowler in a match is _____ (rounded off to one decimal place)



Q11) A symbol stream contains alternate QPSK and 16-QAM symbols. If symbols from this stream are transmitted at the rate of 1 mega-symbols per second, the raw (uncoded) data rate is _____ mega-bits per second (rounded off to one decimal place).

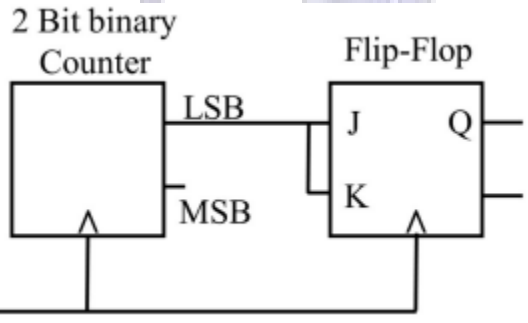
Q12) For the following circuit with an ideal OPAMP, the difference between the maximum and the minimum values of the capacitor voltage (V_C) is _____.





(A) 15 V
(B) 27 V
(C) 13 V
(D) 14 V

Q13) For the circuit shown, the clock frequency is $f0$ and the duty cycle is 25%. For the signal at the Q output of the Flip-Flop, _____.



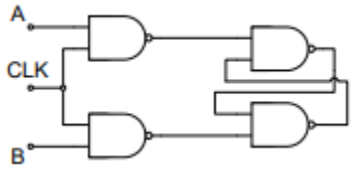
(A) frequency is $f_0/4$ and duty cycle is 50%
(B) frequency is $f_0/4$ and duty cycle is 25%
(C) frequency is $f_0/2$ and duty cycle is 50%
(D) frequency is f_0 and duty cycle is 25%

Q14) Select the CORRECT statement(s) regarding semiconductor devices.
(A) Electrons and holes are of equal density in an intrinsic semiconductor at equilibrium.
(B) Collector region is generally more heavily doped than Base region in a BJT.
(C) Total current is spatially constant in a two terminal electronic device in dark under steady state condition.
(D) Mobility of electrons always increases with temperature in Silicon beyond 300 K

Q15) In a baseband communications link, frequencies upto 3500 Hz are used for signaling. Using a raised cosine pulse with 75% excess bandwidth and for no inter-symbol interference, the maximum possible signaling rate in symbols per second is

(A) 1750
(B) 2625
(C) 4000
(D) 5250

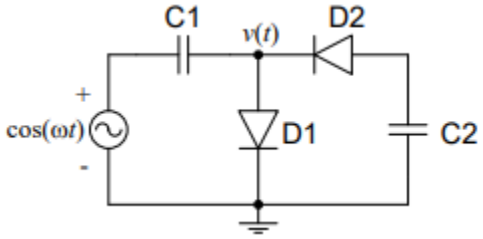
Q16) Consider the given circuit.



In this circuit, the race around
(A) does not occur
(B) occurs when CLK = 0
(C) occurs when CLK = 1 and A = B = 1
(D) occurs when CLK = 1 and A = B = 0

Q17) The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is
(A) 4
(B) 6
(C) 8
(D) 10

Q18) The diodes and capacitors in the circuit shown are ideal. The voltage v(t) across the diode D1 is



(A) cos(*w*t) -1
(B) sin(*w*t)
(C) 1-cos(*w*t)
(D) 1-sin(*w*t)

Q19) A binary symmetric channel (BSC) has a transition probability of 1/8. If the binary transmit symbol X is such that P(X=0) = 9/10, then the probability of error for an optimum receiver will be

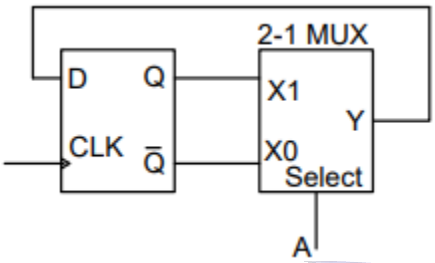
(A) 7/80

(B) 63/80

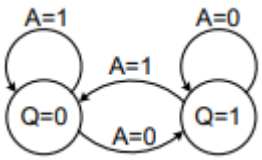
(C) 9/10

(D) 1/10

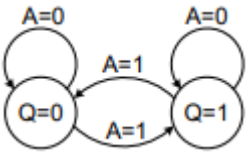
Q20) The state transition diagram for the logic circuit shown is



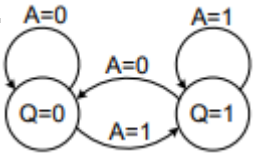
(A)



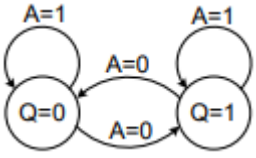
(B)



(C)

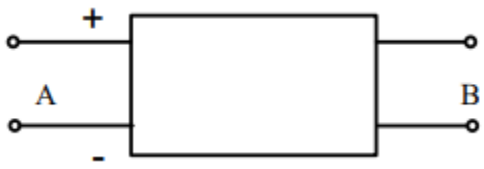


(D)



Common Data for Questions 21 and 22:

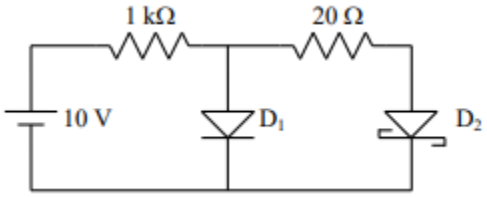
With 10 V dc connected at port A in the linear nonreciprocal two-port network shown below, the following were observed:
(i) 1Ω connected at port B draws a current of 3A
(ii) 2.5Ω connected at port B draws a current of 2A



Q21) With 10 V dc connected at port A, the current drawn by 7Ω connected at port B is
(A) 3/7 A
(B) 5/7 A
(C) 1 A
(D) 9/7 A

Q22) For the same network, with 6 V dc connected at port A, 1Ω connected at port B draws 7/3 A. If 8 V dc is connected to port A, the open circuit voltage at port B is
(A) 6 V
(B) 7 V
(C) 8 V
(D) 9 V

Q23) In the figure, assume that the forward voltage drops of the PN diode D_1 and Schottky diode D_2 are 0.7 V and 0.3 V, respectively. If ON denotes conducting state of the diode and OFF denotes non-conducting state of the diode, then in the circuit



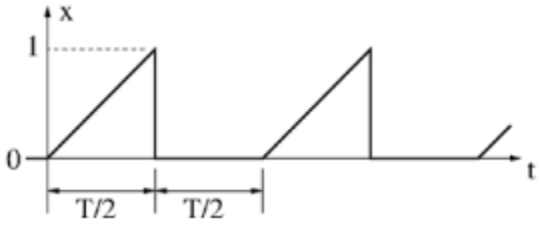
(A) both D_1 and D_2 are ON
(B) D_1 is ON and D_2 is OFF
(C) both D_1 and D_2 are OFF
(D) D_1 is OFF and D_2 is ON

Q24) If fixed positive charges are present in the gate oxide of an n-channel enhancement type MOSFET, it will lead to
(A) a decrease in the threshold voltage
(B) channel length modulation
(C) an increase in substrate leakage current
(D) an increase in accumulation capacitance

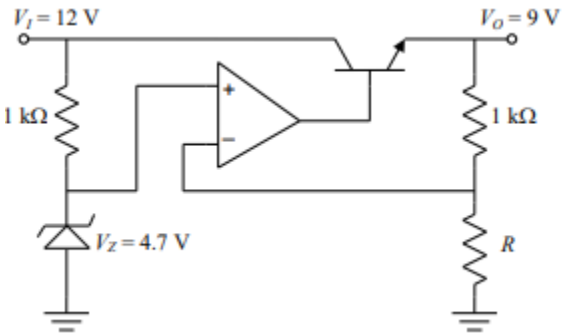
Q25) A good current buffer has
(A) low input impedance and low output impedance
(B) low input impedance and high output impedance
(C) high input impedance and low output impedance
(D) high input impedance and high output impedance

Q26) A Y-network has resistances of 10Ω each in two of its arms, while the third arm has a resistance of 11Ω. In the equivalent Δ-network, the lowest value (in Ω) among the three resistances is _____.

Q27) A periodic variable x is shown in the figure as a function of time. The root-mean-square (rms) value of x is _____.



Q28) In the voltage regulator circuit shown in the figure, the op-amp is ideal. The BJT has V_{BE} = 0.7 V and β = 100, and the zener voltage is 4.7 V. For a regulated output of 9 V, the value of R (in Ω) is _____.



Q29) For a parallel plate transmission line, let *vv* be the speed of propagation and *ZZ* be the characteristic impedance. Neglecting fringe effects, a reduction of the spacing between the plates by a factor of two results in
(A) halving of *v* and no change in *Z*
(B) no changes in *v* and halving of *Z*
(C) no change in both *v* and *Z*
(D) halving of both *v* and z

Q30) A 230 V rms source supplies power to two loads connected in parallel. The first load draws 10 kW at 0.8 leading power factor and the second one draws 10 kVA at 0.8 lagging power factor. The complex power delivered by the source is
(A) (18 + j 1.5) kVA
(B) (18 – j 1.5) kVA
(C) (20 + j 1.5) kVA
(D) (20 – j 1.5) kVA