Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E - ARREAR EXAMINATIONS, NOV / DEC 2023

ELECTIVE
IV
EE5401 & Digital Electronics
(Regulation 2019)

Time: 3hrs Max.Marks: 100

CO 1	To introduce the fundamentals of combinational and sequential digital circuit.
CO 2	To study various number systems and to simplify the mathematical expressions using Boolean functions word problems.
CO 3	To study implementation of combinational circuits using Gates` and MSI Devices.
CO 4	To study the design of various synchronous and asynchronous circuits
CO 5	To introduce digital simulation techniques for development of application oriented logic circuit

BL – Bloom's Taxonomy Levels
(L1 - Remembering, L2 - Understanding, L3 - Applying, L4 - Analyzing, L5 - Evaluating, L6 - Creating)

PART- A (10 x 2 = 20 Marks)
(Answer all Questions)

Q. No	Questions	Marks	CO	BL
1	Simplify the expression using Boolean algebra to minimum literals F = xyz+x'y+xyz'.	2	1	L2
2	What is the 8 bit signed magnitude of the decimal number (-20)?	2	1	L4
3	Design a 2 bit comparator and implement using basic gates	2	2	L1
4	Define PLA with neat diagram	2	2	L1
5	Implement the SR latch using NOR gates and write its truth table.	2	3	L2
6	Write the state reduction techniques and its methods of implementation.	2	3	L1
7	Represent the state transition diagram with an example	2	4	L3
8	Write short notes on race conditions in state transition technique	2	4	L1
9	Differentiate NMOS and CMOS with salient points.	2	5	L4
10	Implement a MUX using behavioral model in VHDL programming technique.	2	5	L3

PART- B (5 x 13 = 65 Marks)
(Restrict to a maximum of 2 subdivisions)

Q. No	Questions	Marks	CO	BL
11 (a) (i)	Simplify the following Boolean function into (a) sum-of-products form and (b) product-of-sums form: F (A, B, C, D) = _(0, 1, 2, 5, 8, 9, 10)	13	1	L2
	OR			
11 (b) (i)	Simplify the following Boolean function, f(W,X,Y,Z)=∑m(2,6,8,9,10,11,14,15) using Quine - McCluskey tabular method.	13	1	L2
12 (a) (i)	Design a combinational circuit that converts a four-bit Gray code to a bit four binary number. Implement the circuit with exclusive-OR gates.	8	2	L3

(ii)	Design a half-subtractor circuit with inputs x and y and outputs Diff and B out. The circuit subtracts the bits x – y and places the difference in D and the borrow in B out.	5	2	L3
	(OR)			
12 (b) (i)	Using a decoder and external gates, design the combinational circuit defined by the following Boolean function F1 = x'yz' + xz	8	2	L3
(ii)	Design a 2 × 4 bit memory using decoder and verify the truth table.	5	2	L3
13 (a) (i)	Using *JK* flip-flops, (a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6	8	3	L3
ii)	Write the state equation for D flip flop.	5	3	L3
	(OR)			
13 (b) (i)	Derive the characteristic equation and excitation equation o f J-K Flip flop.	10	3	L3
(ii)	The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?	3	3	L3
14 (a) (i)	A sequential circuit with two *D* flip-flops *A* and *B*, two inputs, *x* and *y* ; and one output *z* is specified by the following next-state and output equations A(t + 1) = xy' + xB B(t + 1) = xA + xB' z = A (a) Draw the logic diagram of the circuit. (b) List the state table for the sequential circuit. (c) Draw the corresponding state diagram	13	4	L4
	(OR)			
14 (b) (i)	Explain the SR latch as a sequential circuit and implement the truth table as state transition table and draw the corresponding state diagram	13	4	L4
15 (a) (i)	Write short note son RTL and TTL logic families	6	5	L4
(ii)	Write VHDL code to implement a SR flip flop in Dataflow modelling	7	5	L4
	(OR)			
15 (b) (i)	Write a VHDL code to implement the 4 bit synchronous counter	10	5	L4
(ii)	Implement a NAND gate using CMOS technology	3	5	L4

PART- C (1 x 15 = 15 Marks)

(Q.No.16 is compulsory)

Q. No	Questions	Marks	CO	BL
16.	(i) Design a 4 bit adder with carry propagation and verify its truth table with neat diagran ii)Implement the following two Boolean functions with a PLA: F1 = AB'+ AC + A'BC'	10 5	2 5	L5 L5