Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, - Nov/Dec -2023

Information Technology
Semester IV

IT5451 - COMPUTER ARCHITECTURE

(Regulation 2019)

Time:3hrs Max.Marks: 100

CO1	Interpret assembly language instructions.
CO2	Design and analyze ALU circuits.
CO3	Implement a control unit as per the functional specification.
CO4	Design and analyze memory, I/O devices and cache structures for processor.
CO5	Evaluate the performance of computer systems.
CO6	Point out the hazards present in a pipeline and suggest remedies.

BL – Bloom's Taxonomy Levels

(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A (10x2=20Marks)

(Answer all Questions)

Q. No.	Questions	Marks	CO	BL
1	Define Amdahl's law.	2	CO1	L1
2	What are the differences between CISC & RISC processors?	2	CO1	L2
3	Design 4-bit combinational circuit using 4 full adders.	2	CO2	L6
4	What is the difference between the restoring and non restoring method of division?	2	CO2	L2
5	Why is the Wait-for-Memory-Function-Completed step needed when reading from or writing to the main memory?	2	CO3	L4
6	How bit-ORing technique used in Microprogram sequencing?	2	CO3	L4
7	What is SRAM and DRAM?	2	CO4	L1
8	What is interrupt handler? List out the types of interrupts.	2	CO4	L1
9	Classify Parallel Computers.	2	CO5	L1
10	What are the properties of Multi- Core systems?	2	CO5	L2

PART- B (5x 13=65Marks)

(Restrict to a maximum of 2 subdivisions)

Q. No.	Questions	Marks	CO	BL
11 (a)	Explain the basic operstional concepts and list the steps needed to execute the machine instruction, Add LOCA, R0	9	CO1	L3

	Suppose we have two implementation of the same instruction set architecture. Machine "A" has a clock cycle time of 1ns and a CPI of 2.0 for some program, and machine "B" has a clock cycle time of 2ns and a CPI of 1.2 for the same program. Which machine is faster for this program and by how much?	4	CO1	L5
	OR			
11 (b)	List out usage of addressing modes and explain its types.	9	CO1	L3
	Explain Zero, one, two and three addressing instructions with example.	4	CO1	L5
12 (a)	State the principle of carry look ahead adder.	9	CO2	L1
	Consider the binary numbers to be signed, 6-bit values in the 2's complement representation. Perform addition and subtraction, specify whether or not arithmetic overflow occurs. Also convert the operands and results to decimal sign- and-magnitude representation. 100001 011101 ———	4	CO2	L3
	OR			
12 (b)	Explain the logic circuit arrangement to perform Restoring division and state how it can be improved for Non – restoring division technique.	9	CO2	L1
	Solve the following multiplication using Booth's multiplication algorithm. A= 11011 B = 00111 Multiply the following pair of signed 2's complement numbers using bit-pair recoding of the multipliers: A=110101, B=011011.	4	CO2	L3
13 (a)	Write the control sequence for the following instruction considering a single bus organization of the CPU SUB (R3), R2 where R3 is source register and R2 is destination register.	9	CO3	L3
	Draw and explain the Microprogrammed control unit.	4	CO6	L2
	OR			
13 (b)	Explain the instruction execution and hardware organization of a 4-Stage pipeline.	9	CO3	L3
	What are the three types of hazards that cause performance degradation in pipelined processors? Explain them in detail.	4	CO6	L2
14 (a)	What is virtual memory concept? Explain the role of TLB in virtual memory organization.	9	CO4	L2
	Explain associative and set – associative mapping in cache memory.	4	CO4	L2
	OR			
14 (b)	Explain with the block diagram the DMA transfer in a computer system.	9	CO4	L2
	List the functions of I/O interface.	4	CO4	L2

15 (a)	Explain the three parts of scoreboard algorithm and how it works for the below set of instructions.
	LD F6, 34 (R2)
	LD F2, 45 (R3)
	MULT F0, F2 ,F4
	SUBD F8, F6, F2
	DIVD F10, F0, F6
	ADDD F6, F8, F2
		13	CO5	L3

	OR			

15 (b)	Consider the following instructions:
	
	LD F6, 34 (R2)
	LD F2, 45 (R3)
	MULT F0, F2 ,F4
	SUBD F8, F6, F2
	DIVD F10, F0, F6
	ADDD F6, F8, F2
	
	Explain what happens in Tomasulo's algorithm for atleast 5 cycles.
		13	CO5	L3

PART- C (1x 15=15Marks)

(Q.No.16 is compulsory)

Q. No.	Questions	Marks	CO	BL

16.	Consider the following sequence of instructions
	
	Add #20,R0,R1
	
	Mul #3,R2,R3
	
	Add #3,R1,R4
	
	Add R0,R2,R5
	
	In all instructions, the destination operand is given last. Initially, registers R0 and R2 contain 2500 and 100, respectively. These instructions are executed in a computer that has a four-stage pipeline. Assume that the first instruction is fetched in clock cycle 1, and that instruction fetch requires only one clock cycle.
	Draw the pipeline stages to describe the operation.
	Give the contents of the interstage buffers B1,B2 and B3 during clock cycles 2 to 5.
		9	CO6	L5

	Explain in detail the working of a micro programmed control unit to implement the general instruction ADD src,dst in which the source operand can be in any of the five address modes.	**6**	CO3	L3